REMARKS

This Amendment is being submitted in response to the Office Action dated May 28, 2004. Claims 1-6 and 23-48 were pending in the application. In the Office Action, claims 5, 6, 23-26 and 31-33 were withdrawn from consideration, and claims 1-4, 27-30 and 34-48 were rejected. In this Amendment, claims 3, 30, 34, 36, 39, 41, 43 and 46-48 have been amended, and new claims 49-55 have been added. Claims 1-4, 27-30 and 34-55 thus remain for consideration.

Applicants submit that the application is now in condition for allowance and request reconsideration and withdrawal of the rejections in light of the following remarks.

§112 Rejections

Claims 3, 30, 36, 39, 43, 46 and 47 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention

Applicants have amended claims 3, 30, 36, 39, 43, 46 and 47 and submit . that the amendments render the claims compliant with §112. Accordingly, Applicants request withdrawal of the rejections under §112.

§102 and §103 Rejections

In the Official Action, claims 1-4, 35-37 and 42-44 were rejected under 35 U.S.C. 102(b) as being anticipated by Imaoka et al (US 5,426,073).

With respect to base claim 1, the Examiner asserts that "Inaoka et al. [sic] (figs 3's and col. 1-8) discloses the claimed method of manufacturing a semiconductor device ... including selectively grinding or polishing the peripheral portion and the

beveled portion on the main surface side of a target substrate including a semiconductor substrate (1, figs 3a-3b, col. 5 lines 13.17) ... ." his rejection is traversed. However, in the present application, the "beveled portion" is used to denote a portion slanting from the main surface to the side edge of the substrate, and the "peripheral portion" is used to denote a portion adjacent to the slant portion (i.e., beveled portion) at the inner side of the substrate. For example, in FIGS. 3B. 3E, the beveled portion is denoted by "lb," and the peripheral portion is denoted by "la." Thus, contrary to the Examiner's assertion, Imaoka et al does not disclose the claimed feature of grinding or polishing the peripheral portion and the beveled portion, as clearly understood from FIG. 3B. FIG. 3B shows grinding or polishing the side portion alone. Therefore, it is requested that the rejection of claim 1, and claims 2-4 depending from claim 1, under 35 U.S.C. 102(b) be withdrawn.

Imaoka et al. shows another process sequence in FIGS. 7(a)-7(c), though the Examiner has not referred to the process sequence in the Action. In FIG. 7(b), the multiple layer 2 on the peripheral portion and the beveled portion is removed. However, the removal of the multiple layer 2 is attained by selective etching. That is, the multiple layer 2 is etched with selectivity to the substrate 1'. Indeed, Imaoka's col. 8, lines 19-21, describes "Employing a selective etching solution in the etching step, the etching can be terminated on the surface of the original substrate; thus, the wafer diameter does not become smaller ... ." Since the multiple layer 2 is etched with selectivity to the substrate 1', the substrate itself is not removed. Thus, the process sequence of FIGS. 7(a)-7(c) does not disclose grinding or polishing the peripheral portion and the beveled portion, with non-selectivity to the semiconductor substrate.

With respect to base claim 35, the Examiner asserts that "Inaoka et al.

[sic] (figs 3's and col 1-8) discloses the claimed method of manufacturing a semiconductor device ... including selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate (1, figs 3a-3b, col 5 lines 13-17) ... ." However, as pointed out in connection with the asserted claim 1 rejection, Imaoka et al. does not disclose the claimed feature of grinding or polishing the peripheral portion and the beveled portion, as clearly understood from FIG. 3B, and FIG. 3B shows grinding or polishing the side portion alone. Thus, it is requested that the rejection of claims 35, and claims 36 and 37 depending from claim 35, under 35 U.S.C. 102(b) be withdrawn.

Furthermore, as stated with regard to the rejection of claim 1, the process sequence of FIGS. 7(a)-7(c) of Imaoka et al. does not disclose the claimed feature of "grinding or polishing the peripheral portion and the beveled portion, with non-selectivity to the semiconductor substrate."

With respect to base claim 42, the Examiner asserts that "Inaoka et al. [sic] (figs 3's and col 1-8) discloses the claimed method of manufacturing a semiconductor device ... including selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate (1, figs 3a-3b, col 5 lines 13-17) ... ." However, as pointed out above, Imaoka et al. does not disclose the claimed feature of grinding or polishing the peripheral portion and the beveled portion, as clearly understood from FIG. 3B, and FIG. 3B shows grinding or polishing the side portion alone. Thus, withdrawal of the rejection of claim 42, and claims 43 and 44 depending from claim 42, under 35 U.S.C. 102(b) is requested.

Furthermore, as stated with regard to the rejection of claim 1, the process sequence of FIGS. 7(a)-7(c) of Imaoka et al. does not disclose the claimed feature of "grinding or polishing the peripheral portion and the beveled portion, with non-selectivity to the semiconductor substrate."

In the Official Action, claims 27-29, 38-40 and 45-47 were rejected under 35 U.S.C. 103(a) as being unpatentable over Imaoka et al (US 5,426,073) as in view of Jenq (US 5,795,801) and Nakayama (US 6,291,315).

The Examiner admits that Imaoka et al. does not expressly teach selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of the target substrate is carried out after applying an anisotropical dry etching treatment to form a deep and irregular uneven portion in the peripheral portion and the beveled portion of the target substrate, wherein the anisotropic dry etching treatment is carried out to form a trench in the semiconductor substrate and the trench is used for forming a trench capacitor formed on the semiconductor substrate.

The Examiner relies on Jenq (US 5,795,804) and Nakayama et al. to cure these deficiencies of Imaoka et al. However, as argued with respect to claim 1, Imaoka et al. does not disclose the claimed feature of grinding or polishing the peripheral portion and the beveled portion, as clearly understood from FIG. 3B. FIG. 3B shows grinding or polishing the side portion alone. Also, Imaoka's FIG. 7(b) merely shows removing the multiple layer 2 with selectivity to the substrate, and thus does not show the claimed feature of grinding or polishing the peripheral portion and the beveled portion. Thus, even if Imaoka et al, is combined with Jenq and Nakayama et al., the modified process of Imaoka et al. fails to realize the claimed feature of selectively grinding or polishing the

peripheral portion and the beveled portion on the main surface side of the target substrate, as recited in each of claims 27, 38 and 45. Accordingly, it is requested that the rejections of claim 27, and claims 28 and 29 directly/non-directly depending from 27, claim 38, and claims 39 and 40 directly/non-directly depending from 38, and claim 45 and claims 46 and 47 directly/non-directly depending from 45, under 35 U.S.C. 103(a) be withdrawn.

In the Official Action, claims 34, 41 and 48 were rejected under 35 U.S.C. 103(a) as being unpatentable over Imaoka et al (US 5,426,073) in view of Black et al. (US 6,265,314).

The Examiner admits that Imaoka et al. does not expressly teach selectively grinding or polishing the peripheral portion and the beveled portion while a diameter of said semiconductor substrate remains substantially unchanged. The Examiner contends that selectively grinding or polishing the peripheral portion and the beveled portion, while the diameter of the semiconductor substrate remains substantially unchanged is a known technique for removing contaminant from the target substrate, and cites Black et al. as an evidence for the contention.

However, claims 34, 41 and 48 are dependent upon base claims 1, 35 and 42, respectively, and accordingly, the arguments presented against the rejection of the base claims 1, 35 and 42 can be applied fundamentally to this rejection of claim, 34, 41 and 48.That is, as pointed out with respect to the rejection of the base claims 1, 35 and 42, Imaoka et al. does not disclose the claimed feature of grinding or polishing the peripheral portion and the beveled portion, as clearly understood from FIG. 3B. FIG. 3B shows grinding or polishing the side portion alone. Also, Imoaka's FIG. 7(b) merely shows removing the multiple layer 2 with selectivity to the substrate, and thus does not

show the claimed feature of grinding or polishing the peripheral portion and the beveled portion, with non-selectivity to the semiconductor substrate. Thus, Imaoka does not disclose the claimed method including selective grinding or polishing the peripheral portion and the beveled portion of the target substrate, and Black et al, merely teaches a technique to remove contaminant from the target substrate.

In addition, Applicants note that neither Imaoka et al. nor Black teaches the claimed feature of: "to remove the film formed on the peripheral portion and the beveled portion and deep and irregular uneven portion formed in the peripheral portion and the beveled portion," as recited in proposed claim 34. It is therefore unobvious to modify the process of Imaoka et al. by selectively grinding or polishing the peripheral portion and the beveled portion as allegedly taught by Black et al., to remove the film formed on the peripheral portion and the beveled portion and the deep and irregular uneven portion formed in the peripheral portion and the beveled portion. Accordingly, claim 34 is patenatable over Imaoka and Black for at least this reason.

Claims 41 and 48 have been amended in the same manner as claim 34 and are there fore patentable over Imaoka and Black for at least the same reasons discussed in connection with claim 34.

In the Official Action, claim 30 was rejected under 35 U.S C. 103(a) as being unpatentable over Jenq (US 5,795,804) in view of Imaoka et al (US 5,426,073).

The Examiner admits that Jenq does not teach: after depositing the polysilicon film, selectively grinding and polishing a peripheral portion and a beveled portion on the main surface side of the semiconductor substrate wherein the film remaining on the peripheral portion and the beveled portion is removed under a condition

that the film has non-selectivity to the semiconductor substrate. However, the Examiner relies on Imaoka et al. to cure the deficiency of Jenq, and states tat Imaoka et al. teaches selectively grinding and polishing a peripheral portion and a beveled portion on the main surface side of the semiconductor substrate wherein the unwanted films remaining on the peripheral portion and the beveled portion is removed under a condition that the insulating film and the polysilicon film have non-selectivity to the semiconductor substrate.

Jenq discloses a process sequence of forming a DRAM. In Jenq, an insulating film 24 is formed on the main surface of the substrate (FIG. 1), the insulating film 24 and the substrate is anisotropically etched to form a trench 5 in the substrate (FIG. 2), and then polysilicon film 28 is formed on the insulating film 24 and in the trench 5. This is merely part of an ordinary process sequence of forming a DRAM, and the polysilicon film 28 is used as a bottom electrode of a stacked capacitor. Referring to col. 6, lines 39-42, Jenq states that "portions of the N+ doped polysilicon layer 28 also function as the bottom electrodes for the stacked capacitor... ." Obviously, Jenq does not teach forming a polysilicon film on an insulating film in advance of grinding or polishing the peripheral portion and the bevel portion, and then using the polysilicon film for preventing particles (e.g. slurry) from entering the trench when the peripheral portion and the bevel portion are ground or polished.

Furthermore, Jenq does not teach or even suggest the order of processes as claimed in claim 30. Specifically, if in Jenq grinding or polishing the peripheral portion and the bevel portion is to be carried out, the grinding or polishing would be carried out before, not after, forming the polysilicon layer 28. Thus, Jenq does not contemplate

preventing particles, typically slurry, from entering the trench when the peripheral portion and the bevel portion are grinded or polished. To the contrary, in claim 30, grinding or polishing the peripheral portion and the beveled portion is carried out after the polysilicon is deposited. The claimed feature of "after depositing the polysilicon film, selectively grinding or polishing a peripheral portion and a beveled portion" is a patently distinctive feature. Jenq makes no mention on grinding or polishing the peripheral portion and the beveled portion. Hence, it is unreasonable to expect one skilled in the art to combine Jenq with Imaoka et al. to realize the claimed feature of "after depositing the polysilicon film, selectively grinding or polishing the peripheral portion and the beveled portion," and the rejection of claim 30 should be withdrawn.

Applicants submit that all of the claims now pending in the application are in condition for allowance, which action is earnestly solicited.

It is submitted that these claims, as originally presented, are patentably distinct over the prior art cited by the Examiner, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes to these claims, as presented herein, are not made for the purpose of patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these changes are made simply for clarification and to round out the scope of protection to which Applicants are entitled.

Statements appearing above with respect to the disclosures in the cited references represent the present opinions of the Applicants' undersigned attorney and, in the event that the Examiner disagrees with any such opinions, it is respectfully requested

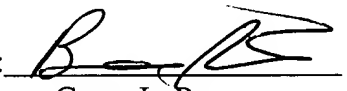
that the Examiner specifically indicate those portions of the respective reference providing the basis for a contrary view.

If any issues remain, or if the Examiner has any further suggestions, he/she is invited to call the undersigned at the telephone number provided below.

The Examiner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account No. 50-0320.

The Examiner's consideration of this matter is gratefully acknowledged.

Respectfully submitted,
FROMMER LAWRENCE & HAUG LLP

By: 

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